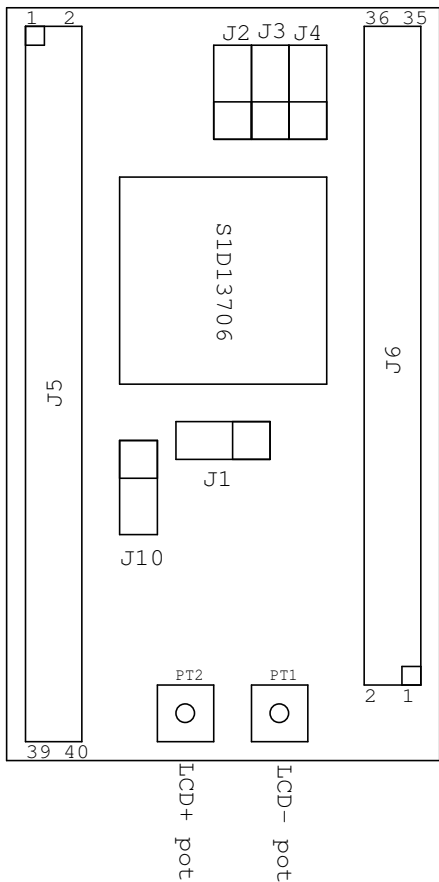


Processor bus interface
(or IOTester interface)

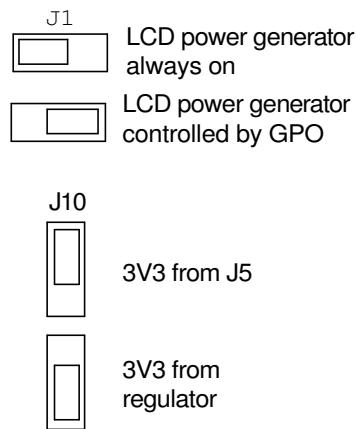
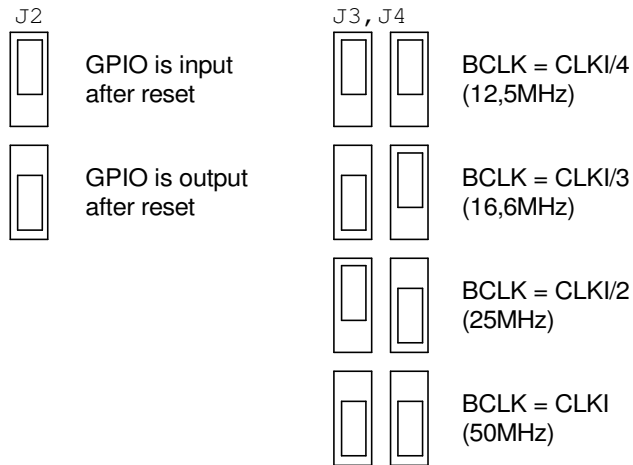


LCD / TFT display bus interface

J6 Display bus signals, Possible S1D13706 LCD bus configurations (via software)

J6 Pin Name	Monocrom 4-bit	Monocrom 8-bit	Color STN 4-bit	Color STN Format 1 8-bit	Color STN Format 2 8-bit	Color STN 16-bit	Color TFT 9-bit	Color TFT 12-bit	Color TFT 18-bit	Sharp HR-TFT 18-bit	Epson D-TFD 18-bit
36 PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT	PWMOUT
35 CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT	CVOUT
34 GPO	GPO	GPO	GPO	GPO	GPO	GPO	GPO	GPO	GPO	MOD	GPO
33 GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	YSCLD
32 GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	DD_P1
31 GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	RES
30 GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	SPL	FRS
29 GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	REV	FR
28 GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	CLS	YSCL
27 GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	PS	XINH
26 FPDAT17	0	0	0	0	0	0	0	0	B0	B0	B0
25 FPDAT16	0	0	0	0	0	0	0	0	B1	B1	B1
24 FPDAT15	0	0	0	0	0	D15	0	B0	B2	B2	B2
23 FPDAT14	0	0	0	0	0	D14	0	0	G0	G0	G0
22 FPDAT13	0	0	0	0	0	D13	0	0	G1	G1	G1
21 FPDAT12	0	0	0	0	0	D12	0	G0	G2	G2	G2
20 FPDAT11	0	0	0	0	0	D11	0	0	R0	R0	R0
19 FPDAT10	0	0	0	0	0	D10	0	0	R1	R1	R1
18 FPDAT9	0	0	0	0	0	D9	0	R0	R2	R2	R2
17 FPDAT8	0	0	0	0	0	D8	B0	B1	B3	B3	B3
16 FPDAT7	D3	D7	D3	D7	D7	D7	B1	B2	B4	B4	B4
15 FPDAT6	D2	D6	D2	D6	D6	D6	B2	B3	B5	B5	B5
14 FPDAT5	D1	D5	D1	D5	D5	D5	G0	G1	G3	G3	G3
13 FPDAT4	D0	D4	D0	D4	D4	D4	G1	G2	G4	G4	G4
12 FPDAT3	0	D3	0	D3	D3	D3	G2	G3	G5	G5	G5
11 FPDAT2	0	D2	0	D2	D2	D2	R0	R1	R3	R3	R3
10 FPDAT1	0	D1	0	D1	D1	D1	R1	R2	R4	R4	R4
9 FPDAT0	0	D0	0	D0	D0	D0	R2	R3	R5	R5	R5
8 DRDY	MOD	MOD	MOD	FPSHIFT2	MOD	MOD	DRDY	DRDY	DRDY	DRDY	DRDY
7 FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT
6 FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE
5 FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME
4 3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3
3 GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
2 -LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD	-LCD
1 +LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD	+LCD

Jumper settings



Different display module vendors often use different names for the same signals:
 FPFRAME is also called Frane Sync, or Vertical Sync clock
 FPLINE is also called Line Sync, or Horizontal Sync clock
 FPSHIFT is also called Clock, Data clock
 DRDY is also called Data Enable

Title		
S1D13706 Prototype Board		
Size A4	Document Number Jumper settings & display bus config	Rev 3
Date:	Tuesday, July 19, 2005	Sheet 2 of 2